

Microprocessor-Compatible, Real-Time Clock

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Intersil's silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $1/100$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{ACC}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power Down Detector eliminates the need for external components to support the battery back-up function. When a power down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

Features

- 8-Bit, μ P Bus Compatible
 - Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll Over During Read
- Full Calendar with Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less than 300ns
- 4 Programmable Crystal Oscillator Frequencies Over Industrial Temperature Range
- 3 Programmable Crystal Oscillator Frequencies Over Military Temperature Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 1.2 μ A Typical at 3.0V and 32kHz Crystal

Applications

- Portable and Personal Computers
- Data Logging
- Industrial Control Systems
- Point Of Sale

***For complete Rochester ordering guide, please refer to page 2
Please consult factory for specific package availability***

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ICM7170

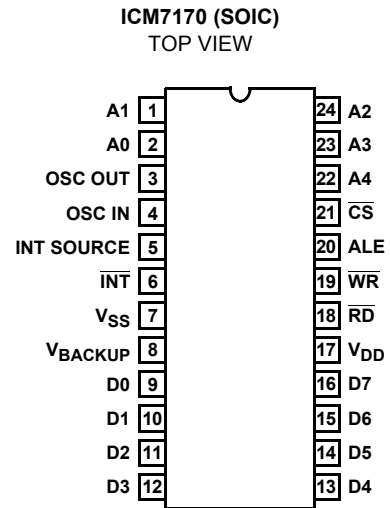
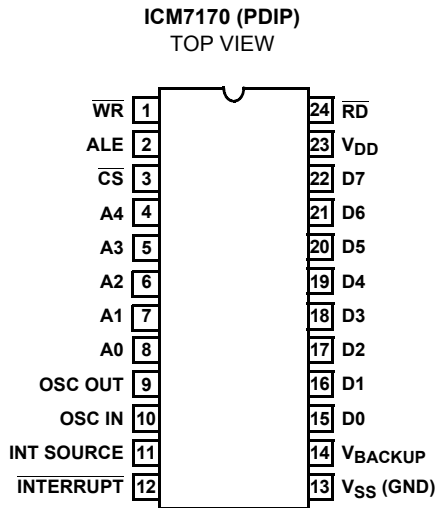
Rochester Ordering Guide

**Most products can also be offered as RoHS compliant, designated by a -G suffix. Please contact factory for more information.*

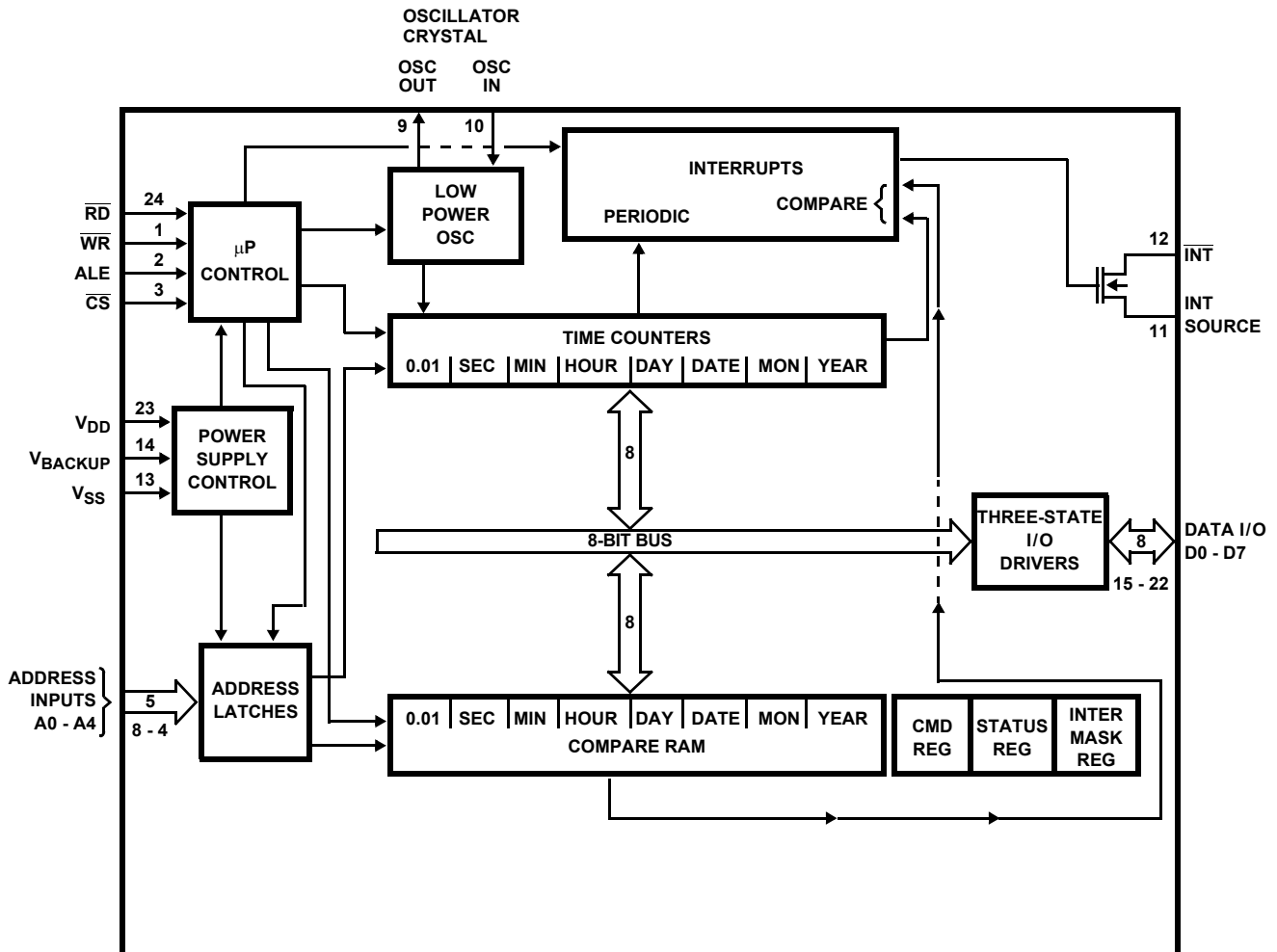
Rochester Part Number	Intersil Part Number	Package	Temperature
ICM7170AIBG	ICM7170AIBG	SOP-24, Plastic	-40° to +85°C
ICM7170AIBGT	ICM7170AIBGT	SOP-24, Plastic	-40° to +85°C
ICM7170AIDG	ICM7170AIDG	CDIP-24	-40° to +85°C
ICM7170AIPG	ICM7170AIPG	PDIP-24	-40° to +85°C
ICM7170AMDG	ICM7170AMDG	CDIP-24	-55° to +125°C
ICM7170IBG	ICM7170IBG	SOP-24, Plastic	-40° to +85°C
ICM7170IBGT	ICM7170IBGT	SOP-24, Plastic	-40° to +85°C
ICM7170IDG	ICM7170IDG	CDIP-24	-40° to +85°C
ICM7170IPG	ICM7170IPG	PDIP-24	-40° to +85°C
ICM7170MDG	ICM7170MDG	CDIP-24	-55° to +125°C

ICM7170

Pinouts



Functional Block Diagram



ICM7170

Absolute Maximum Ratings $T_A = 25^{\circ}\text{C}$

Supply Voltage	+8.0V
Power Dissipation (Note 1)	.500mW
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering 10s)	300°C
Input Voltage (Any Terminal) (Note 2)	$V_{DD} + 0.3\text{V}$ to $V_{SS} - 0.3\text{V}$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	50	N/A
SOIC Package	75	N/A
Maximum Junction Temperature		
Plastic Package		150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
- Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Electrical Specifications $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{DD} + 5\% \pm 10\%$, $V_{BACKUP} = V_{DD}$, $V_{SS} = 0\text{V}$ Unless Otherwise Specified All I_{DD} specifications include all input and output leakages (ICM7170 and ICM7170A)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Range, V_{DD}	$f_{OSC} = 32\text{kHz}$	1.9	-	5.5	V
	$f_{OSC} = 1, 2, 4\text{MHz}$	2.6	-	5.5	V
Standby Current, $I_{STBY}(1)$	$f_{OSC} = 32\text{kHz}$ Pins 1 - 8, 15 - 22 and 24 = V_{DD}		1.2	20.0	μA
	$V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0\text{V}$ For ICM7170A See General Notes 5		1.2	5.0	μA
Standby Current, $I_{STBY}(2)$	$f_{OSC} = 4\text{MHz}$ Pins 1 - 8, 15 - 22 and 24 = V_{DD} $V_{DD} = V_{SS}$; $V_{BACKUP} = V_{DD} - 3.0\text{V}$	-	20	150	μA
Operating Supply Current, $I_{DD}(1)$	$f_{OSC} = 32\text{kHz}$, Read/Write Operation at 100Hz	-	0.3	1.2	mA
Operating Supply Current, $I_{DD}(2)$	$f_{OSC} = 32\text{kHz}$, Read/Write Operation at 1MHz	-	1.0	2.0	mA
Input Low Voltage (Except Osc.), V_{IL}	$V_{DD} = 5.0\text{V}$	-	-	0.8	V
Input High Voltage (Except Osc.), V_{IH}	$V_{DD} = 5.0\text{V}$	2.4	-	-	V
Output Low Voltage (Except Osc.), V_{OL}	$I_{OL} = 1.6\text{mA}$	-	-	0.4	V
Output High Voltage Except <u>INTERRUPT</u> (Except Osc.), V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
Input Leakage Current, I_{IL}	$V_{IN} = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
Three-State Leakage Current (D0 - D7), $I_{OL}(1)$	$V_O = V_{DD}$ or V_{SS}	-10	0.5	+10	μA
Backup Battery Voltage, $V_{BATTERY}$	$f_{OSC} = 1, 2, 4\text{MHz}$	2.6	-	$V_{DD} - 1.3$	V
Backup Battery Voltage, $V_{BATTERY}$	$f_{OSC} = 32\text{kHz}$	1.9	-	$V_{DD} - 1.3$	V
Leakage Current <u>INTERRUPT</u> , $I_{OL}(2)$	$V_O = V_{DD}$		0.5	10	μA
	INT SOURCE Connected to V_{SS}	-			
Capacitance D0 - D7, $C_{I/O}$		-	8	-	pF
Capacitance A0 - A4, $C_{ADDRESS}$		-	6	-	pF

ICM7170

AC Electrical Specifications $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{DD} = +5\text{V} \pm 10\%$, $V_{\text{BACKUP}} = V_{DD}$,
 $D0 - D7$ Load Capacitance = 150pF , $V_{IL} = 0.4\text{V}$, $V_{IH} = 2.8\text{V}$, Unless Otherwise Specified

PARAMETER	MIN	MAX	UNITS
READ CYCLE TIMING			
READ to DATA Valid, t_{RD}	-	250	ns
ADDRESS Valid to DATA Valid, t_{ACC}	-	300	ns
READ Cycle Time, t_{CYC}	400	-	ns
Read High Time, t_{RH}	150	-	ns
$\overline{\text{RD}}$ High to Bus Three-State, t_{RH}	-	25	ns
ADDRESS to READ Set Up Time, t_{AS}	50	-	ns
ADDRESS HOLD Time After READ, t_{AR}	0	-	ns
WRITE CYCLE TIMING			
ADDRESS Valid to WRITE Strobe, t_{AD}	50	-	ns
ADDRESS Hold Time for WRITE, t_{WA}	0	-	ns
WRITE Pulse Width, Low, t_{WL}	100	-	ns
WRITE High Time, t_{WH}	300	-	ns
DATA IN to WRITE Set Up Time, t_{DW}	100	-	ns
DATA IN Hold Time After WRITE, t_{WD}	30	-	ns
WRITE Cycle Time, t_{CYC}	400	-	ns
MULTIPLEXED MODE TIMING			
ALE Pulse Width, High, t_{LL}	50	-	ns
ADDRESS to ALE Set Up Time, t_{AL}	30	-	ns
ADDRESS Hold Time After ALE, t_{LA}	30	-	ns

Timing Diagrams

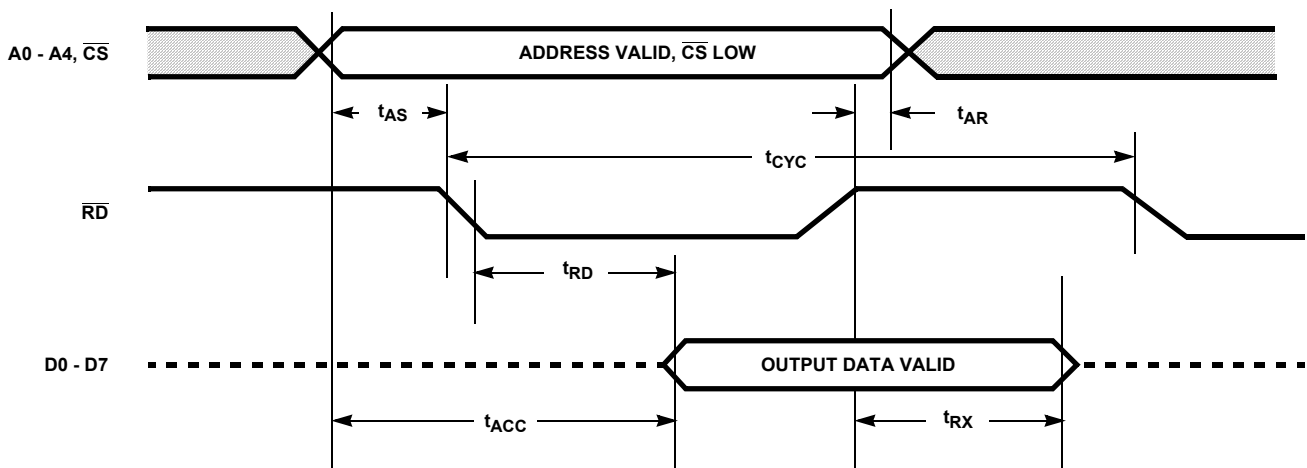


FIGURE 1. READ CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH} , $\overline{\text{WR}} = V_{IH}$)

Timing Diagrams (Continued)

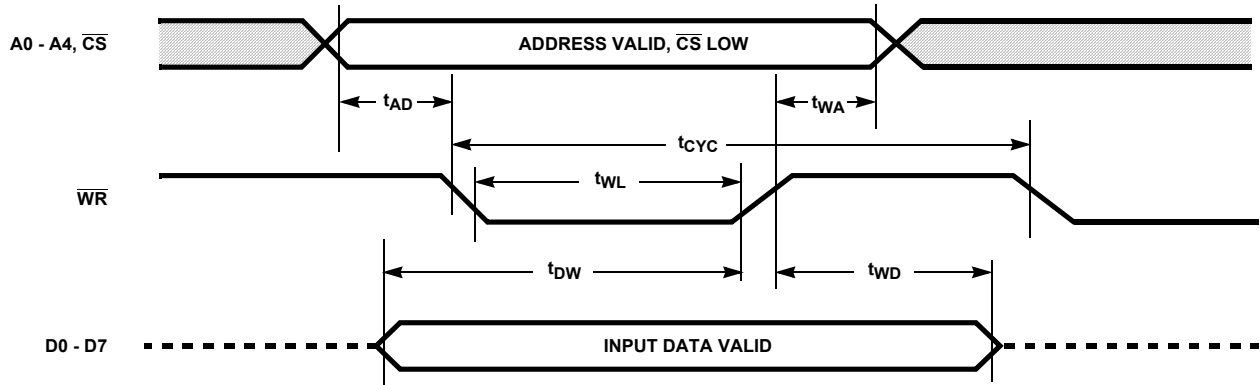


FIGURE 2. WRITE CYCLE TIMING FOR NON-MULTIPLEXED BUS ($ALE = V_{IH}$, $\overline{RD} = V_{IH}$)

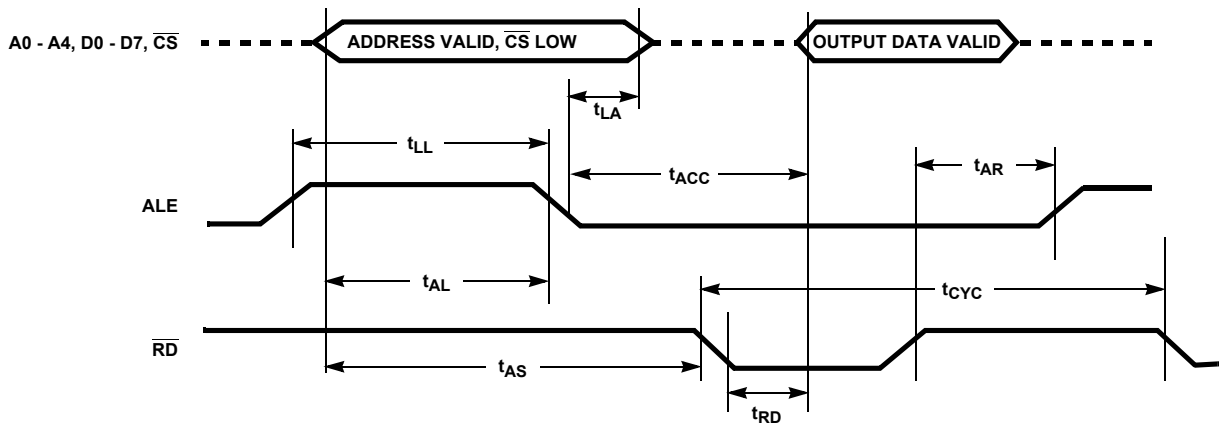


FIGURE 3. READ CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{WR} = V_{IH}$)

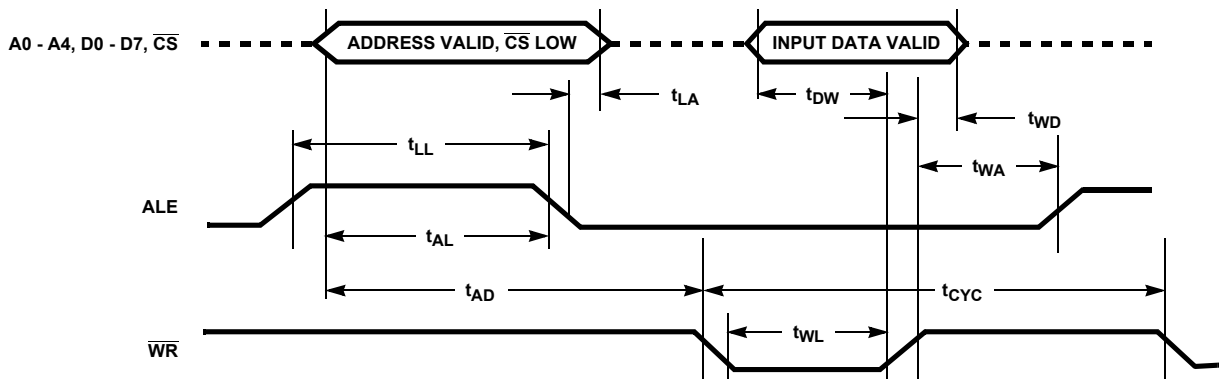


FIGURE 4. WRITE CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{RD} = V_{IH}$)

ICM7170

Pin Descriptions

SIGNAL	PIN NUMBER	SOIC PIN NUMBER	DESCRIPTION
\overline{WR}	1	19	Write Input
ALE	2	20	Address Latch Enable Input
\overline{CS}	3	21	Chip Select Input
A4-A0	4 - 8	22 - 2	Address Inputs
OSC OUT	9	3	Oscillator Output
OSC IN	10	4	Oscillator Input
INT SOURCE	11	5	Interrupt Source
$\overline{INTERRUPT}$	12	6	Interrupt Output
V _{SS} (GND)	13	7	Digital Common
V _{BACKUP}	14	8	Battery Negative Side
D0 - D7	15 - 22	9 - 16	Data I/O
V _{DD}	23	17	Positive Digital Supply
\overline{RD}	24	18	Read Input

TABLE 1. COMMAND REGISTER FORMAT

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Normal/Test Mode	Interrupt Enable	Run/Stop	12/24 Hour Format	Crystal Frequency	Crystal Frequency

TABLE 2. COMMAND REGISTER BIT ASSIGNMENTS

D5	TEST BIT	D4	INTERRUPT ENABLE	D3	RUN/STOP	D2	24/12 HOUR FORMAT	D1	D0	CRYSTAL FREQUENCY
0	Normal Mode	0	Interrupt disabled	0	Stop	0	12-Hour Mode	0	0	32.768kHz
1	Test Mode	1	Interrupt enable	1	Run	1	24-Hour Mode	0	1	1.048576MHz
								1	0	2.097152MHz
								1	1	4.194304MHz

TABLE 3. ADDRESS CODES AND FUNCTIONS

ADDRESS						FUNCTION	DATA								VALUE
A4	A3	A2	A1	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	00	Counter-1/100 seconds	-								0 - 99
0	0	0	0	1	01	Counter-hours	-	-	-						0 - 23
						12 Hour Mode	†	-	-	-					1 - 12
0	0	0	1	0	02	Counter-minutes	-	-							0 - 59
0	0	0	1	1	03	Counter-seconds	-	-							0 - 59
0	0	1	0	0	04	Counter-month	-	-	-	-					1 - 12
0	0	1	0	1	05	Counter-date	-	-	-						1 - 31
0	0	1	1	0	06	Counter-year	-								0 - 99
0	0	1	1	1	07	Counter-day of week	-	-	-	-					0 - 6
0	1	0	0	0	08	RAM-1/100 seconds	M								0 - 99
0	1	0	0	1	09	RAM-hours	-	M	-						0 - 23
						12 Hour Mode	†	M	-	-					1 - 12
0	1	0	1	0	0A	RAM-minutes	M	-	.	.					0 - 59
0	1	0	1	1	0B	RAM-seconds	M	-	.	.					0 - 59
0	1	1	0	0	0C	RAM-month	M	-	-	-					1 - 12
0	1	1	0	1	0D	RAM-date	M	-	-						1 - 31
0	1	1	1	0	0E	RAM-year	M								0 - 99

TABLE 3. ADDRESS CODES AND FUNCTIONS (Continued)

ADDRESS						FUNCTION	DATA								VALUE
A4	A3	A2	A1	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	1	1	1	1	0F	RAM-day of week	M	-	-	-	-				0 - 6
1	0	0	0	0	10	Interrupt Status and Mask Register	+								
1	0	0	0	1	11	Command register	-	-							

NOTES:

Addresses 10010 to 11111 (12h to 1Fh) are unused.

‘+’ Unused bit for interrupt Mask Register, MSB bit for interrupt Status Register.

‘-’ Indicates unused bits.

‘†’ AM/PM indicator bit in 12 hour format Logic “0” indicates AM, logic “1” indicates PM.

‘M’ Alarm compare for particular counter will be enabled if bit is set to logic “0”.

TABLE 4. INTERRUPT AND STATUS REGISTERS FORMAT

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
NOT USED	DAY	HOURL	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
	← Periodic Interrupt Mask Bits →						Alarm/Compare Mask Bit
INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL INTERRUPT	DAY	HOURL	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
Periodic and Alarm Flags	← Periodic Interrupt Flags →						Alarm Compare Flag

Detailed Description

Oscillator

The ICM7170 has an onboard CMOS Pierce oscillator with an internally regulated voltage supply for maximum accuracy, stability, and low power consumption. It operates at any of four popular crystal frequencies: 32.768kHz, 1.046576MHz, 2.097152MHz, and 4.194304MHz (Note 1). The crystal should be designed for the parallel resonant mode of oscillation. In addition to the crystal, 2 or 3 load capacitors are required, depending on the circuit topology used.

The oscillator output is divided down to 4000Hz by one of four divider ratios, determined by the two frequency selection bits in the Command Register (D0 and D1 at address 11H). This 4000Hz is then divided down to 100Hz, which is used as the clock for the counters.

Time and calendar information is provided by 8 consecutive, programmable counters: 100ths of, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format with 8 bits per digit. See Table 3 for address information. Any unused bits are held to a logic “0” during a read and ignored during a write operation.

NOTE:

- 4.194304MHz is not available over military temperature range.

Alarm Compare RAM

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 10ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM

word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate ‘M’ bit in Compare RAM should be set to logic “1”.

The ‘M’ bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 3 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100Hz, 10Hz, once per second, once per minute, once per hour, or once per day. The 100Hz and 10Hz interrupts have instantaneous errors of $\pm 2.5\%$ and $\pm 0.15\%$ respectively. This is because non-integer divider circuitry is used to generate these signals from the crystal frequency, which is a power of 2. The time average of these errors over a 1 second period, however, is zero. Consequently, the 100Hz or 10Hz interrupts are not suitable as an aid in tuning the oscillator; the 1 second interrupt must be used instead.

See General Notes, Note 6.

The periodic interrupts can occur concurrently and in addition to alarm interrupts. The periodic interrupts are controlled by bits in the interrupt mask register, and are enabled by setting the appropriate bit to a “1” as shown in Table 4. Bits D1 through D6 in the mask register, in conjunction with bits D1 through D6 of the status register, control the generation of interrupts according to Figure 5.

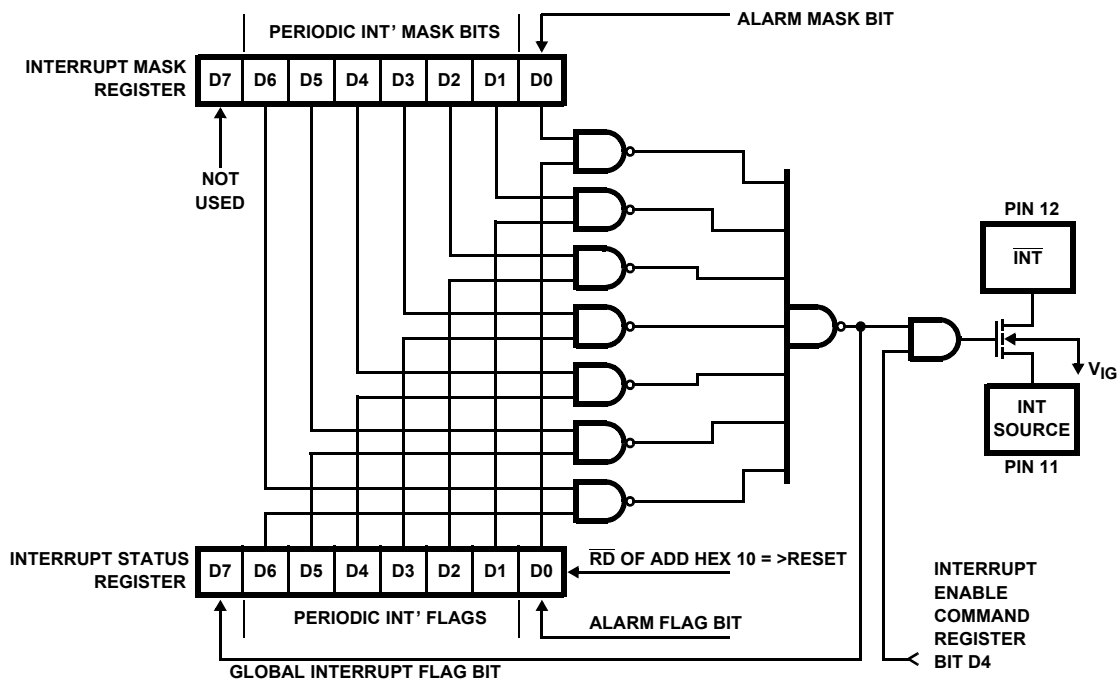


FIGURE 5. INTERRUPT OUTPUT CIRCUIT

The interrupt status register, when read, indicates the cause of the interrupt and resets itself on the rising edge of the RD signal. When any of the counters having a corresponding bit in the status register increments, that bit is set to a “1” regardless of whether the corresponding bit in the interrupt mask register is set or not.

Consequently, when the status register is read it will always indicate which counters have increments and if an alarm compare occurred, since the last time it was read. This requires some special software considerations. If a slow interrupt is enabled (i.e., hourly or daily), the program must always check the slowest interrupt that has been enabled first, because all the other lower order bits in the status register will be set to “1” as well.

Bit D7 is the global interrupt bit, and when set to a “1”, indicates that the ICM7170 did indeed generate a hardware interrupt. This is useful when other interrupting devices in addition to the ICM7170 are attached to the system microprocessor, and all devices must be polled to determine which one generated the interrupt.

See General Notes, Note 6.

Interrupt Operation

The Interrupt Output N-channel MOSFET (Figure 4) is enabled whenever both the Interrupt Enable bit (D4 of the Command Register) and a mask bit (D0 - D6 of the Interrupt Mask Register) are set. The transistor is turned ON when a flag bit is set that corresponds to one of the set mask bits. This also sets the Global Interrupt Flag Bit (D7 of the Interrupt Status Register). It is turned OFF when the Interrupt Status Register is

read. An interrupt can occur in both the operational and standby modes of operation.

Since system power is usually applied between V_{DD} and V_{SS} , the user can connect the Interrupt Source (pin 11) to V_{SS} . This allows the Interrupt Output to turn on only while system powers applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power Down Detector

The ICM7170 contains an on-chip power down detector that eliminates the need for external components to support the battery-backup switchover function, as shown in Figure 6. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin is less than approximately 1.0V (the V_{TH} of the N-channel MOSFET), the data bus I/O buffers in the ICM7170 are automatically disabled and the chip cannot be read or written to. This prevents random data from the microprocessor being written to the clock registers as the power supply is going down.

Actual switchover to battery operation occurs when the voltage on the V_{BACKUP} pin is within $\pm 50\text{mV}$ of V_{SS} . This switchover uncertainty is due to the offset voltage of the CMOS comparator that is used to sense the battery voltage. During battery backup, device operation is limited to timekeeping and interrupt generation only, thus achieving micro-power current drain. If an external battery-backup switch-over circuit is being used with the ICM7170, or if standby battery operation is not required, the V_{BACKUP} pin should be pulled up to V_{DD} through a 2K resistor.

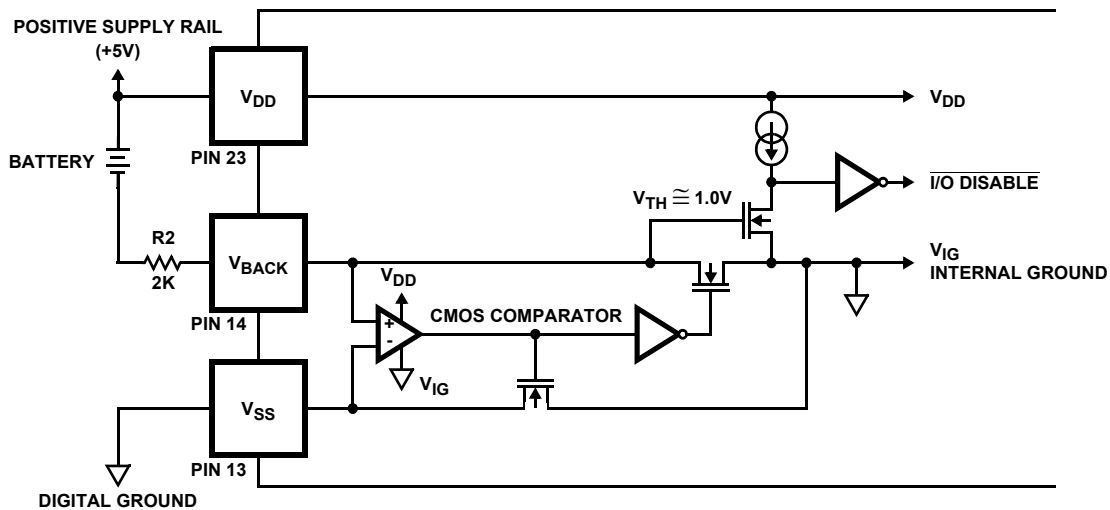


FIGURE 6. SIMPLIFIED ICM7170 BATTERY BACKUP CIRCUIT

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is transferred into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again. If a \overline{RD} signal is wider than 0.01s, 100Hz counts will be ignored.

Control Lines

The \overline{RD} , \overline{WR} , and \overline{CS} signals are active low inputs. Data is placed on the bus from counters or registers when \overline{RD} is a logic "0". Data is transferred to counters or registers when \overline{WR} is a logic "0". \overline{RD} and \overline{WR} must be accompanied by a logical "0" \overline{CS} as shown in Figures 2 and 3. The ICM7170 will also work satisfactorily with \overline{CS} grounded. In this mode, access to the ICM7170 is controlled by \overline{RD} and \overline{WR} only.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0 - A4 to the data lines D0 - D4. To address the chip, the address is placed on the bus and ALE is strobed. On the

falling edge, the address and \overline{CS} information is read into the address latch and buffer. \overline{RD} and \overline{WR} are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD} .

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz counter directly to the oscillator's output.

Oscillator Considerations

Load Design: A new oscillator load configuration, shown in Figure 7, has been found that eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

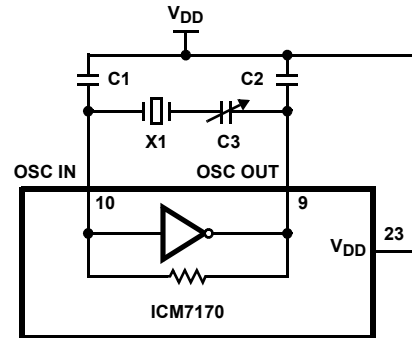


FIGURE 7. NEW OSCILLATOR CONFIGURATION

Two conditions must be met for best oscillator performance: the capacitive load must be matched to both the inverter and crystal to provide the ideal conditions for oscillation, and the resonant frequency of the oscillator must be adjustable to the desired frequency. In the original design (Figure 8), these two goals were often at odds with each other; either the oscillator was trimmed to frequency by detuning the load circuit, or stability was increased at the expense of absolute frequency accuracy.

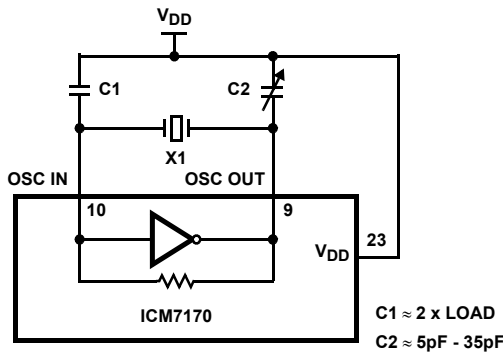


FIGURE 8. ORIGINAL OSCILLATOR CONFIGURATION

The new load configuration (Figure 6) allows these two conditions to be met independently. The two load capacitors, C1 and C2, provide a fixed load to the oscillator and crystal. C3 adjusts the frequency that the circuit resonates at by reducing the effective value of the crystal's motional capacitance, C0. This minute adjustment does not appreciably change the load of the overall system, therefore, stability is no longer affected by tuning. Typical values for these capacitors are shown in Table 5. C1 and C2 must always be greater than twice the crystal's recommended load capacitance in order for C3 to be able to trim the frequency. Some experimentation may be necessary to determine the ideal values of C1 and C2 for a particular crystal.

TABLE 5. TYPICAL LOAD CAPACITOR VALUES

CRYSTAL FREQUENCY	LOAD CAPS (C1, C2)	TRIMMER CAP (C3)
32kHz	33pF	5 - 50pF
1MHz	33pF	5 - 50pF
2MHz	25pF	5 - 50pF
4MHz	22pF	5 - 100pF

This three capacitor tuning method will be more stable than the original design and is mandatory for 32kHz tuning fork crystals: without it they may leap into an overtone mode when power is initially applied.

The original two-capacitor circuit (Figure 8) will continue to work as well as it always has, and may continue to be used in applications where cost or space is a critical consideration. It is also easier to tune to frequency since one end of the trimmer capacitor is fixed at the AC ground of the circuit (V_{DD}), minimizing the disturbance cause by contact between the adjustment tool and the trimmer capacitor. Note that in both configurations the load capacitors are connected between the oscillator pins and V_{DD} - do not use V_{SS} as an AC ground.

Layout: Due to the extremely low current (and therefore high impedance) design of the ICM7170s oscillator, special attention must be given to the layout of this section. Stray capacitance should be minimized. Keep the oscillator traces

on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the ICM7170 OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential sources of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Oscillator Tuning

Trimming the oscillator should be done indirectly. Direct monitoring of the oscillator frequency by probing OSC IN or OSC OUT is not accurate due to the capacitive loading of most probes. One way to accurately trim the ICM7170 is by turning on the 1 second periodic interrupt and trimming the oscillator until the interrupt period is exactly one second. This can be done as follows:

1. Turn on the system. Write a 00H to the Interrupt Mask Register (location 10H) to clear all interrupts.
2. Set the Command Register (location 11H) for the appropriate crystal frequency, set the Interrupt Enable and Run/Stop bits to 1, and set the Test bit to 0.
3. Write a 08H to the Interrupt Mask Register to turn on the 1s interrupt.
4. Write an interrupt handler to read the Interrupt Status Register after every interrupt. This resets the interrupt and allows it to be set again. A software loop that reads the Interrupt Status Register several times each second will accomplish this also.
5. Connect a precision period counter capable of measuring 1s within the accuracy desired to the interrupt output. If the interrupt is configured as active low, trigger on the falling edge. If the interrupt is active high, trigger on the rising edge. Be sure to measure the period between when the transistor turns ON, and when the transistor turns ON a second later.
6. Adjust C3 (C2 for the two-capacitor load configuration) for an interrupt period of exactly 1.000000 seconds.

Application Notes

Digital Input Termination During Backup

To ensure low current drain during battery backup operation, none of the digital inputs to the ICM7170 should be allowed to float. This keeps the input logic gates out of their transition region, and prevents crossover current from flowing which will shorten battery life. The address, data, \overline{CS} , and ALE pins should be pulled to either V_{DD} or V_{SS} , and the \overline{RD} and \overline{WR} inputs should be pulled to V_{DD} . This is necessary whether the internal battery switchover circuit is used or not.

IBM/PC Evaluation Circuit

Figure 9 shows the schematic of a board that has been designed to plug into an IBM PC/XT (Note 1) or compatible computer. In this example \overline{CS} is permanently tied low and access to the chip is controlled by the \overline{RD} and \overline{WR} pins. These signals are generated by U1, which gates the IBM's \overline{IOR} and \overline{IOW} with a device select signal from U3, which is

ICM7170

functioning as an I/O block address decoder. DS1 selects the interrupt priority.

U5 is used to isolate the ICM7170 from the PC databus for test purposes. It is only required on heavily-loaded TTL databuses - the ICM7170 can drive most TTL and CMOS databuses directly.

Since the IBM PC/XT (Note 1) requires a positive interrupt transition, the ICM7170's interrupt output transistor has been configured as a source follower. As a source follower, the interrupt output signal will swing between 0V and 2.5V.

When trimming the oscillator, the frequency counter must be triggered on the rising edge of the interrupt signal.

TABLE 6.

BATTERIES	CRYSTALS		
Panasonic	Saronix	32kHz	NTF3238
Rayovac	Statek	32kHz	CX - 1V
	Seiko	2MHz	GT - 38

NOTE:

1. IBM, IBM PC, and IBM XT are trademarks of IBM Corp.

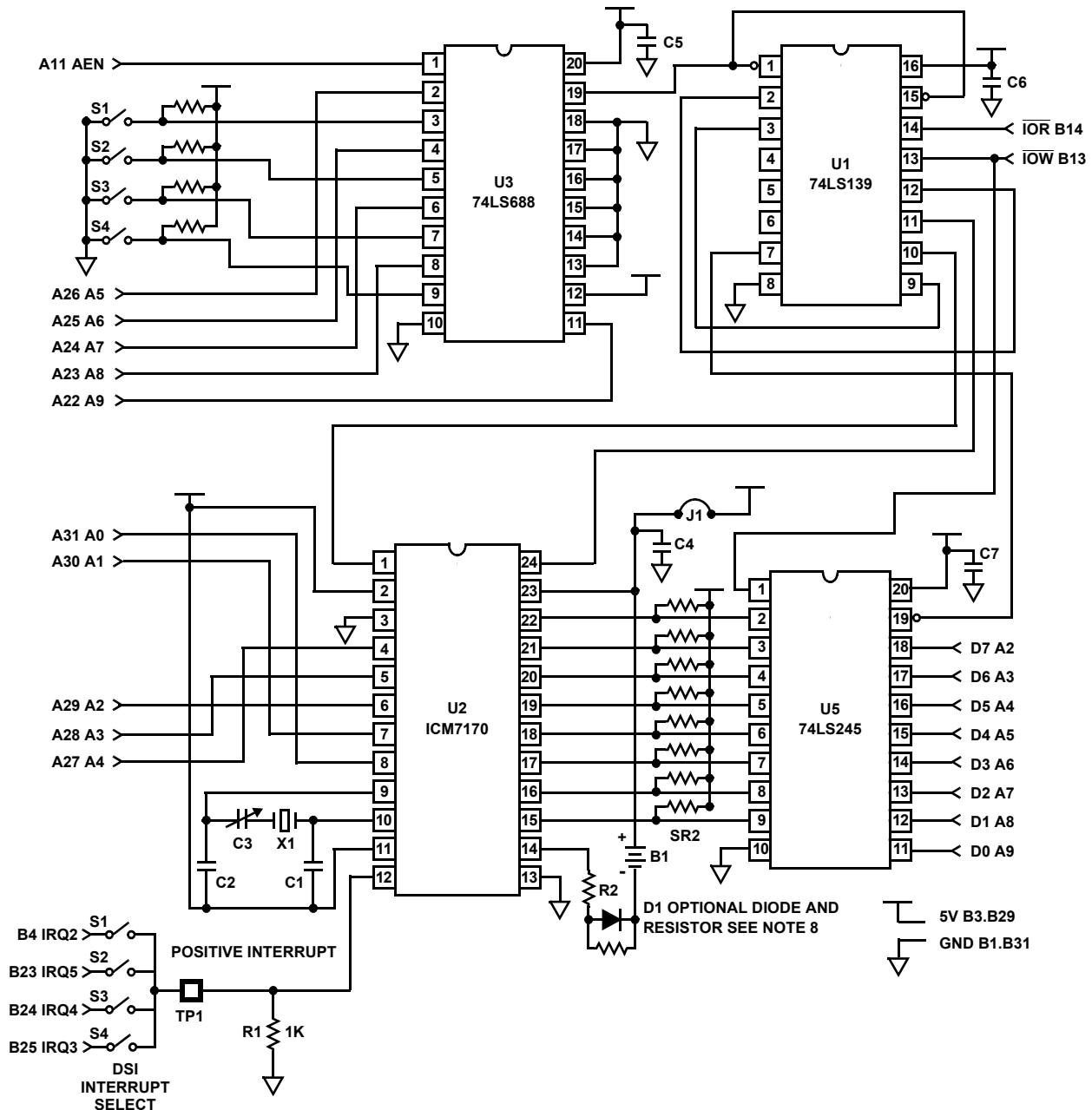
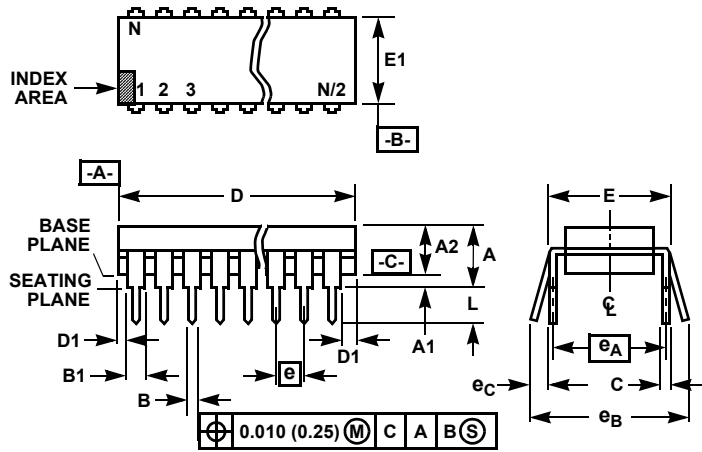


FIGURE 9. IBM PC INTERFACE FOR ICM7170Y

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

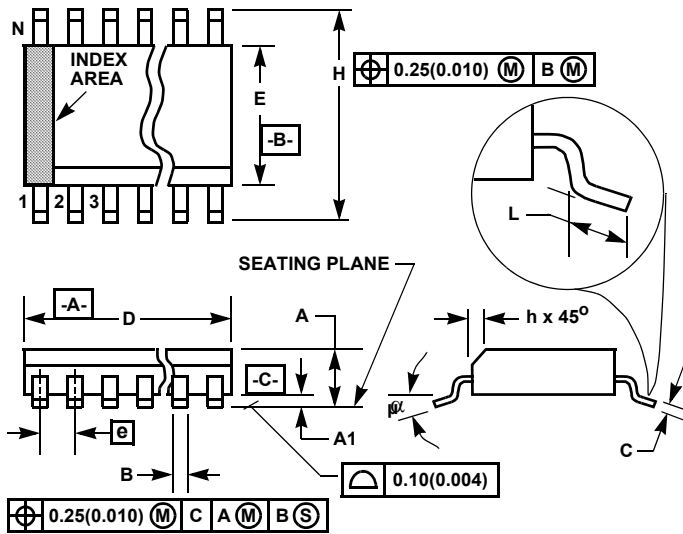
**E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

Rev. 0 12/93

ICM7170

Small Outline Plastic Packages (SOIC)



M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rochester Electronics guarantees performance of its semiconductor products to the original OEM specifications. "Typical" values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing. Rochester Electronics reserves the right to make changes without further notice to any specification herein.